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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,029	08/26/2003	Kenneth J. Kledzik	044148-004100	2417

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EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,029	KLEDZIK ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the ball-grid array and wherein the ball-grid array of the first and second IC packages are conductively bonded, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 35-36, 38-43,45-47, 49-51, 54-62, and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vakilian (US 6,160,718, newly cited, hereinafter, Vakilian) and in view of Kim (US 6,069,025, newly cited, hereinafter, Kim.)

In regard to claim 35, 40, 45, 51, 57, 62, and 65, in fig. 5, Vakilian discloses an electronic circuit module comprising:

a carrier 12 comprising a first integrated circuit mounting location comprising a first mounting pad array, a second integrated circuit mounting location disposed on the opposite side of said first mounting pad array comprising a second mounting pad array, a ball-grid array 22, and a carier interface; wherein said first and second mounting pad arrays are conductively coupled with said carrier interface,

first and second integrated circuit packages 20, each comprising a package body comprising an integrated circuit chip and; and

a printed circuit board 32 having at least one interconnection pad array coupled to circuitry on said printed circuit and conductively bonded to said carder interface.

Vakilian, however, does not expressly disclose using ball-grid array to connect the chip to the carrier. It should be noted that using ball-grid array to provide electrical

connections is widely used in semiconductor packaging since the array provides better electrical contacts and in some cases it facilitates the connection process. For instance, Kim, in fig. 6, discloses an analogous package and further teaches using ball-grid array 67 to connect the IC chips 62 to the carrier 61.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the widely available connection method as taught by Kim in order to provide better connections.

In regard to claims 36, 47, and 64, wherein individual mounting pads of said first mounting pad array are coupled to individual mounting pads of said second mounting pad array by means of conductive links within said carrier. See Vakilian's fig. 6.

In regard to claims 38, 41, and 49, 58-59, and 66, wherein said carrier further comprises a carrier body with a recess for receiving at least a portion of said first and second integrated circuit packages. See Vakilian's fig. 5.

In regard to claims 39 and 50, see Kim's fig. 6.

In regard to claims 42-43, 55-56, and 60-61, wherein said ball- grid array on said carrier comprises balls configured in at least single row. See Vakilian's fig. 5.

In regard to claim 46, the combination further discloses a printed circuit board having at least one interconnection pad array coupled to circuitry on said printed circuit and conductively bonded to said carrier interface. See Vakilian's fig. 5.

In regard to claim 54, the combination further comprises at least a second carrier conductively bonded with said printed circuit board. See Vakilian's fig. 5.

In regard to claim 67, the combination further comprises:

a second integrated circuit package comprising:

a second integrated circuit chip, and

a second ball-grid array;

wherein said interconnection pad array on said printed circuit board comprises interconnection pads beneath the recess in said carrier and said second bail-grid array on said second integrated circuit package are conductively bonded to said interconnection array beneath the recess in said carrier on said printed circuit board. See also Vakilian's fig. 5.

3. Claims 37, 44, 48, and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vakilian and Kim as applied to claims 35-36, 38-43, 45-47, 49-51, 54-62, and 64-67 above, and further in view of Shim et al. (US 6,683,377, previously cited, and hereinafter, Shim.)

In regard to claims 37, 44 and 48, the above combination discloses all of the claimed limitations as mentioned above except the carrier comprises a flexible polymeric film. It should be noted that polymeric material is widely used in the art of semiconductor package to protect metal interconnections from exposing to the outside to prevent oxidation or electrical short circuit.

For instance, Shim discloses a package that includes polymeric film 10 as an insulating film to protect core layer 11, for example (see also, col. 2, lines 40-44 and figs. 1B-4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to include an insulating layer, specifically, polymeric layer, in order to protect metal connection devices.

In regard to claims 52-53, see the above discussions regarding to claims 35 and 38.

4. Claims 44 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vakilian and Kim as applied to claims 35-36, 39-40, 42-43, 45-46, 49-53, 54-58, 59-62, and 64-67 above, and further in view of Herrell et al. (US 6,828,666, previously cited, hereinafter, Herrell.)

In regard to claims 44 and 63, the combination of Vakilian and Kim discloses all of the claimed limitations as mentioned above except the substrate is a ceramic ball-grid array. Herrell discloses an analogous package including multiple chips mounted on a ceramic ball-grid array in order to reduce the difference in thermal coefficient between the substrate and the dies.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to substitute the ceramic substrate as taught by Herrell in order to take the advantage as mentioned above.

Response to Arguments

5. Applicant's arguments with respect to claims 35-67 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
Primary Examiner
October 25, 2006